

3U8S CompactPCI 32-Bit Backplane
User Manual

PICMG 2.0 R3.0

P/N: CPCI20-38VLR_32-A1



TEL : +886-2-22690567

FAX : +886-2-22690327

www.mapsuka.com.tw

E-Mail : mapsuka@mapsuka.com.tw

Dec. 03, 2009

1. Key Features :

- Conforms to PICMG 2.0 R3.0
- Supports Hot Swap feature of PICMG 2.1 R2.0
- Conforms to PICMG 2.9 R1.0
- VI/O are user selectable to a +5V or +3.3V
- All signal lines characteristic impedance are set to 65 Ω
- FR4 material PCB
- 2 m/m HM connector

2. Mechanical

The CompactPCI CPC120-38VLR_32-A1 backplane is a 10-layer PCB with 3U (128.7 mm) tall, 3.2 mm thick, 181.88 mm width. Two layers are dedicated ground layers. The backplanes are attached to the subrack using a series of screws along the top and bottom edges of the backplanes.

3. Backplane Pattern Connection Specification

Slot1 (S1) : System (Left side)

Slot2 (S2) : Peripheral

Slot3 (S3) : Peripheral

Slot4 (S4) : Peripheral

Slot5 (S5) : Peripheral

Slot6 (S6) : Peripheral

Slot6 (S7) : Peripheral

Slot6 (S8) : Peripheral

3.1 CLK line

Slot No.	S1	S2	S3	S4	S5	S6	S7	S8
CLK No.	System	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5	CLK6

3.2 GNT/REQ line

Slot No.	S1	S2	S3	S4	S5	S6	S7	S8
GNT/	System	GNT0/	GNT1/	GNT2/	GNT3/	GNT4/	GNT5/	GNT6/

REQ		REQ0	REQ1	REQ2	REQ3	REQ4	REQ5	REQ6
-----	--	------	------	------	------	------	------	------

3.3 IDSEL line

Slot No.	S1	S2	S3	S4	S5	S6	S7	S8
IDSEL	System	AD31	AD30	AD29	AD28	AD27	AD26	AD25

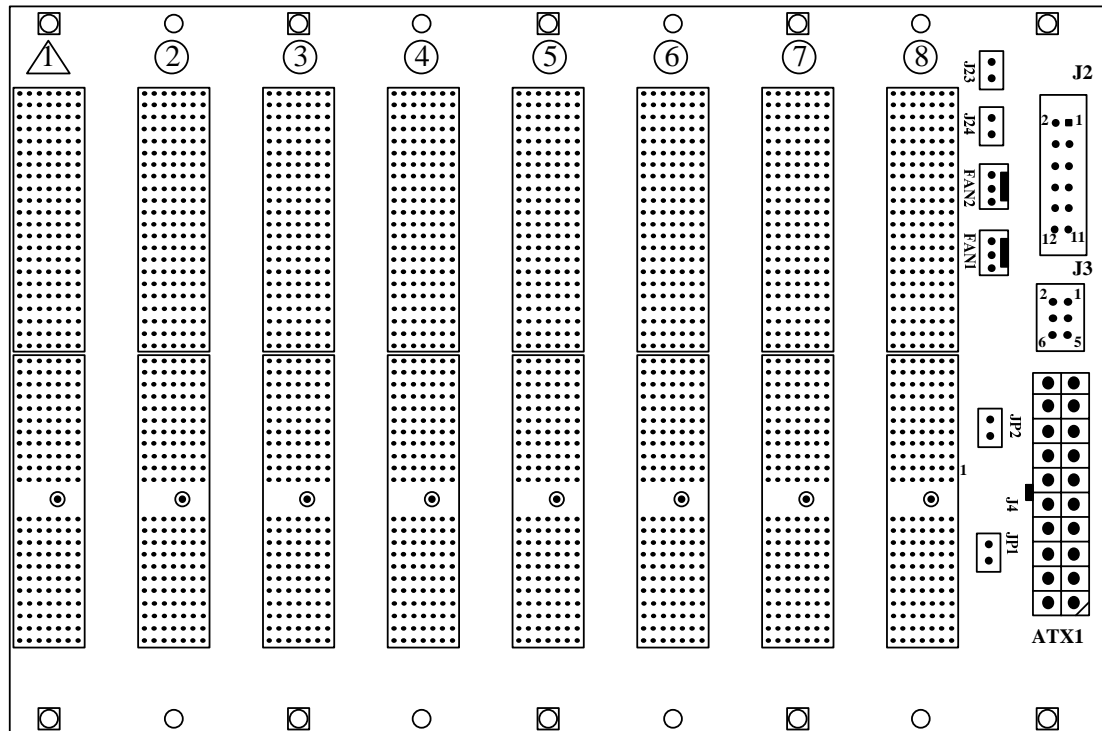
3.4 Interrupt line

Slot No.	S1	S2	S3	S4	S5	S6	S7	S8
Interrupt line	INTA#	INTD#	INTC#	INTB#	INTA#	INTD#	INTC#	INTB#
	INTB#	INTA#	INTD#	INTC#	INTB#	INTA#	INTD#	INTC#
	INTC#	INTB#	INTA#	INTD#	INTC#	INTB#	INTA#	INTD#
	INTD#	INTC#	INTB#	INTA#	INTD#	INTC#	INTB#	INTA#

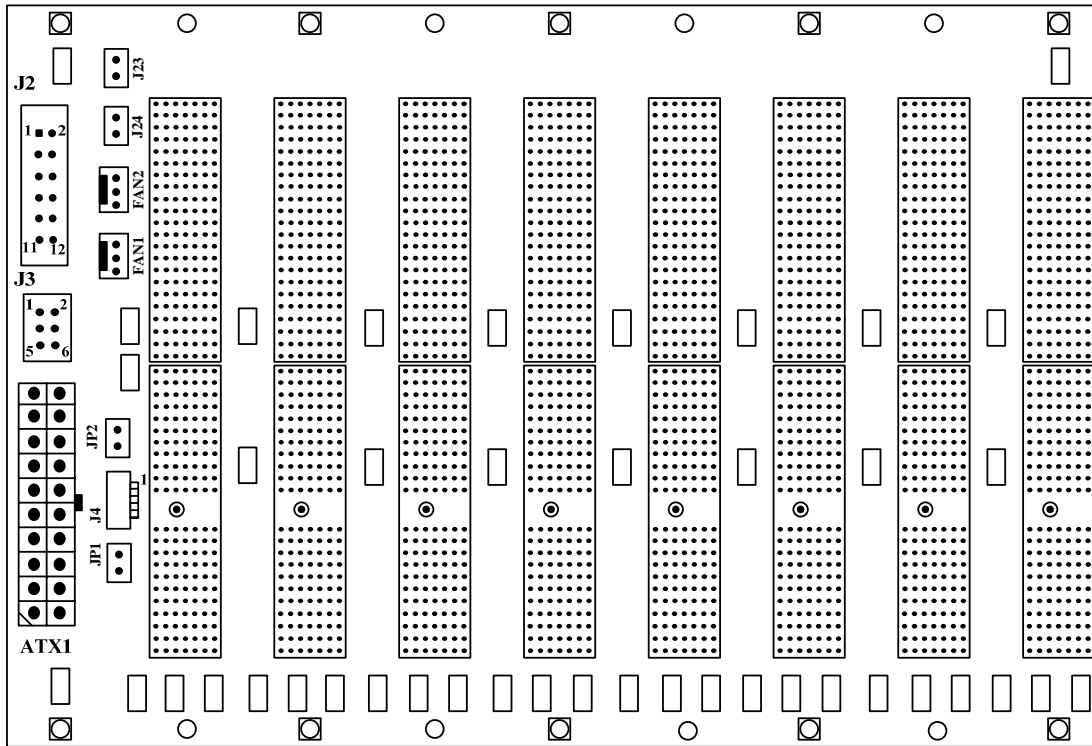
4. Connectors and Jumpers

The relative position of connectors and jumpers on the backplane are shown as the following Figures.

Front Side



Rear Side



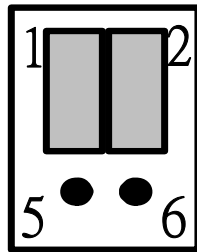
4.1 J2 connector

Alarm connector : Providing all of power supply and Fan status on the backplane for remote monitoring.

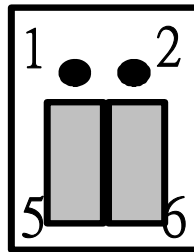
Pin	1	2	3	4	5	6	7	8	9	10	11	12
Power	Fan1	+12V	Fan2	+5V	-	GND	-	+3.3V	-	-12V	-	GND

4.2 J3 connector

VI/O Selector



+3.3V



+5V

4.3 J4 connector

IPMB Extension connector.

Pin	1	2	3	4	5
Signals	IPMB_SCL	GND	IPMB_SDA	IPMB_PWR	IPMB_ALERT

4.4 J23 connector

Connecting a Push-button switch for system reset.

4.5 J24 connector

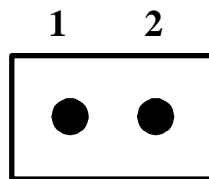
DEG signal of System Slot for remote monitoring.

4.6 JP1 connector

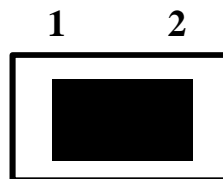
Power switch connector.

4.7 JP2 jumper

M66EN, the 66MHz Enabling line, is defined as GND for 33 MHz backplane.



66 MHz



33 MHz

4.8 ATX1 power connector

Pin	Power	Pin	Power
1	+3.3V	11	+3.3V
2	+3.3V	12	-12v
3	GND	13	GND
4	+5V	14	PSON#
5	GND	15	GND
6	+5V	16	GND
7	GND	17	GND
8	FAL-	18	-5V
9	DEG-	19	+5V
10	+12V	20	+5V

5. Backplane Pin Assignment Table

Table 5.1 CompactPCI System Slot P1 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
24	GND	AD[1]	+5V	VI/O	AD[0]	ACK64#	GND
23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	VI/O	AD[11]	AD[10]	GND
19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	VI/O	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	GND	TRDY#	GND
J1-12~14 Keying Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	VI/O	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ0#	GND	+3.3V	CLK0	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	PCI_RST#	GND	GNT0#	GND
4	GND	IPMB_PWR	HEALTHY#	VI/O	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND	TCK	+5V	TMS	TDO1	TDI1	GND
1	GND	+5V	-12V	TRST#	+12V	+5V	GND
Pin	Z	A	B	C	D	E	F

Table 5.2 CompactPCI System Slot P2 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
22	GND	GND	GND	GND	GND	GA0	GND
21	GND	CLK6	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND
20	GND	CLK5	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND
19	GND	GND	GND	BP(I/O)	BP(I/O)	SMB_ALERT	GND
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND

17	GND	BP(I/O)	BP(I/O)	PRST#	REQ6#	GNT6#	GND
16	GND	BP(I/O)	BP(I/O)	DEG#	GND	BP(I/O)	GND
15	GND	BP(I/O)	BP(I/O)	FAL#	REQ5#	GNT5#	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	VI/O	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	GND	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND
Pin	Z	A	B	C	D	E	F

Table 5.3 CompactPCI Peripheral Slot P1 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
24	GND	AD[1]	+5V	VI/O	AD[0]	ACK64#	GND
23	GND	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	GND	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	GND	+3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	VI/O	AD[11]	AD[10]	GND
19	GND	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	GND	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	VI/O	STOP#	LOCK#	GND
15	GND	+3.3V	FRAME#	IRDY#	GND	TRDY#	GND
J1-12~14 Keying Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	VI/O	AD[25]	AD[24]	GND

7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	+3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	PCI_RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	VI/O	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	+5V	INTD#	GND
2	GND	TCK	+5V	TMS	TDO	TDO	GND
1	GND	+5V	-12V	TRST#	+12V	+5V	GND
Pin	Z	A	B	C	D	E	F

Table 5.4 CompactPCI Peripheral Slot P2 Connector Pin assignments

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
20	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
19	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
17	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
16	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
15	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND
Pin	Z	A	B	C	D	E	F